SEVENTH CAUSE OF ACTION

(Unfair Competition And Trade Secret Misappropriation Under Lanham Act §§ 44(b) and (i))

(By TSMC-NA and WaferTech Against SMIC Ltd.)

80. Paragraphs 1-79 above are incorporated herein by reference.

81. The United States and the People's Republic of China are parties to the Paris Convention for the Protection of Industrial Property (Stockholm 1967) ("Paris Convention"), which is a convention or treaty relating to trademarks, trade or commercial names, and the repression of unfair competition.

82. The United States and the People's Republic of China are signatories to the Memorandum of Understanding Between the Government of the United States of America and the Government of the People's Republic of China on the Protection of the Intellectual Property (1992), in which the PRC acknowledged that unfair competition under the Paris Convention encompassed trade secret misappropriation.

83. Plaintiffs TSMC-NA and WaferTech are citizens of the United States entitled under Section 44(i), 15 U.S.C. §1126(i) to the benefits described in Section 44(b) of the Lanham Act, 15 U.S.C. § 1126(b).

84. The country of origin of SMIC Ltd. is the People's Republic of China, and thus SMIC Ltd. is a person described in Section 44(b) of the Lanham Act, 15 U.S.C. § 1126(b).

85. By its actions as set forth above, SMIC Ltd. has injured and is injuring TSMC-NA and WaferTech by intentionally engaging in acts of unfair competition contrary to honest practices in industrial or commercial matters, including by acquiring, using, and disclosing trade secrets without the consent of TSMC-NA and WaferTech in a manner contrary to honest commercial practices.

86. As a proximate result of SMIC Ltd.'s acts of unfair competition, TSMC-NA and WaferTech have suffered or will suffer damages in an amount to be determined at trial.

87. TSMC-NA and WaferTech are entitled under Sections 44(b) and (i) of the Lanham Act, 15 U.S.C. §§ 1126(b) and (i), to all remedies available under the California

Uniform Trade Secret Act, the California Bus. & Prof. Code § 17200 *et. seq.*, and common law unfair competition.

88. TSMC-NA and WaferTech are further entitled to the remedies provided under the Lanham Act for infringement of marks, insofar as they may be appropriate to repress SMIC Ltd.'s acts of unfair competition, including, without limitation recovery of SMIC Ltd.'s profits, any damages sustained by TSMC-NA or WaferTech, treble damages, injunctive relief, and costs. This is an exceptional case, such that SMIC is also liable for attorneys fees.

EIGHTH CAUSE OF ACTION

(Unfair Competition Under Cal. Bus. & Prof. Code § 17200 *et seq.*)

(By all Plaintiffs Against Both Defendants)

89. Paragraphs 1-88 above are incorporated herein by reference.

90. As alleged above, Defendants have wrongfully misappropriated, conspired to misappropriate, and have attempted wrongfully to misappropriate, Plaintiffs' trade secrets in violation of the Uniform Trade Secrets Act, California Civil Code Sections 3426 *et seq.* Defendants have further violated and conspired to violate the Federal Economic Espionage Act of 1996, 18 U.S.C. § 1832, which makes it a crime to steal trade secrets. With respect to section 1832, acts in furtherance of the offense were committed by Defendants in the United States.

91. By violating and by conspiring to violate both California Civil Code Sections 3426, *et seq.*, 18 U.S.C. § 1832, and the Lanham Act, §§ 44(b) and (i), Defendants have engaged in unlawful, unfair, and/or fraudulent business practices within the meaning of California Business and Professions Code Section 17200.

92. The natural, probable, and foreseeable result of SMIC's conduct has been and will continue to be to injure Plaintiffs' businesses, to impose substantial expenses on Plaintiffs to counteract that conduct, and to injure and damage Plaintiffs in other ways.

93. Defendants have used this unfair business practice to their advantage, taking customers and substantial lucrative contracts away from Plaintiffs, and causing substantial price erosion as to other TSMC products and sales. Defendants have unfairly profited, and will continue to unfairly benefit, as a result of these acts of unfair competition.

94. Unless restrained and enjoined, Defendants will continue irreparably to harm Plaintiffs. Plaintiffs have no adequate remedy at law, and money damages cannot fully compensate them for the injury to their business. Plaintiffs are thus entitled to injunctive relief prohibiting Defendants from disclosing or continuing to use Plaintiffs' proprietary trade-secrets to further its competing enterprise.

PRAYER FOR RELIEF

TSMC respectfully requests the following relief:

1. A judgment that SMIC has infringed the asserted patents;

2. Damages for SMIC's willful infringement of the asserted patents, including treble damages, interest, and costs;

3. A permanent injunction against SMIC's infringement of the asserted patents;

4. Preliminary and permanent injunctive relief pursuant to which SMIC and SMIC Americas, and their employees, or representatives, and all persons acting in concert or participating with them are commanded, enjoined, or restrained, directly or indirectly, by any means whatsoever, as follows:

   a. From incorporating into, or using Plaintiffs' trade secrets and other proprietary information to manufacture, offer to sell, or sell products or services incorporating, using, or made using Plaintiffs' trade secrets, or to disclose Plaintiffs' trade secrets and proprietary information;

   b. Immediately to preserve and return to Plaintiffs or to this Court (i) all information, including trade secret and other confidential or proprietary information improperly acquired from Plaintiffs; (ii) all materials (in paper, electronic, or any other form) containing any, or derived from, such trade secrets or other confidential or proprietary information; and (iii) all copies of such materials; and

   c. To turn over to the Court any proceeds they have received from the misappropriation of Plaintiffs' trade secrets, to be held in constructive trust until the conclusion of this litigation;

5. General damages, restitution and/or disgorgement arising from SMIC's trade-secret misappropriation, along with lost interest thereon, as well as doubled

damages, according to proof;

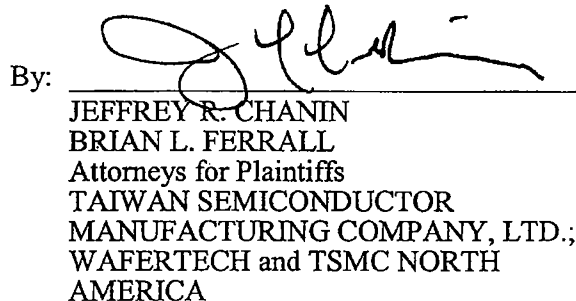
6. Attorney's fees and costs, based upon a finding that this is either an exceptional case under 35 U.S.C. § 285, or 15 U.S.C. § 1117(a)(3); and/or that SMIC has engaged in willful and malicious misappropriation of Plaintiffs' trade secrets under Cal. Civ. Code § 3426.4;

7. Costs of court; and

8. All such other relief that the court deems just and proper.

Dated: December 19, 2003

KEKER & VAN NEST, LLP



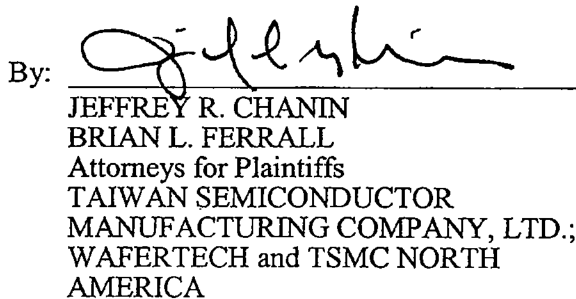
By: ______________________
JEFFREY R. CHANIN
BRIAN L. FERRALL
Attorneys for Plaintiffs
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.; WAFERTECH and TSMC NORTH AMERICA

DEMAND FOR JURY TRIAL

Under Rule 38(b) of the Federal Rules of Civil Procedure and Local Rule 3-6 of the United States District Court for the Northern District of California, Plaintiffs hereby demand a trial by jury of all issues properly triable by jury.

Dated: December 19, 2003

KEKER & VAN NEST, LLP

By: 

JEFFREY R. CHANIN
BRIAN L. FERRALL
Attorneys for Plaintiffs
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.; WAFERTECH and TSMC NORTH AMERICA

CERTIFICATION OF INTERESTED ENTITIES OR PERSONS

Pursuant to Civil L.R. 3-16, the undersigned certifies that the following listed persons, associations of persons, firms, partnerships, corporations (including parent corporations) or other entities (i) have a financial interest in the subject matter in controversy or in a party to the proceeding, or (ii) have a non-financial interest in that subject matter or in a party that could be substantially affected by the outcome of this proceeding:

Development Fund of the Executive Yuan
KoninklijkevPhilips Electronics N.V.
Global UniChip Corp.
Systems on Silicon Manufacturing Co., Pte. Ltd.
Vanguard International Semiconductor Corp.
TSMC Japan K.K.
TSMC International Investments, Ltd.
TSMC Technology, Inc.
TSMC Development, Inc.
TSMC Europe B.V.
TSMC Partners, Ltd.

Dated: December 19, 2003

KEKER & VAN NEST, LLP

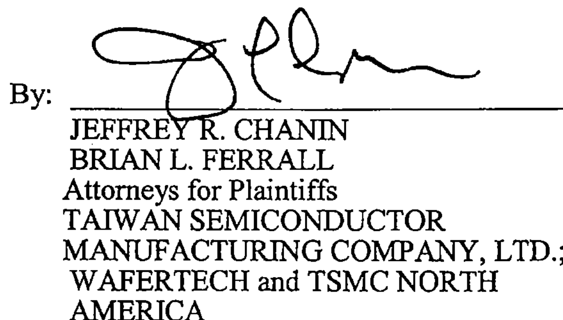
By: 

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Exhibit A

(1)

Marco Mora
To: clairc@ms4.hinet.net
Subject: Need Information

Hi Katy,

I heard from Richard that you are coming to Shanghai to help us on interviewing people. Welcome! We have more than 600 applications already and other 300 are coming. You will be quite busy, but this is very promise because at least we do not have any manpower recruiting issue.

I need a help from you to pull-out some of the information from WSMC/ TSMC. I think you can some help from your people or eventually you can ask to Shinmo.

- **Process flows**

  - Detailed process flow of 0.35um Logic (Part 1006) from Fab-1, including process tar and equipment type
  - Detailed process flow of 0.28um ROM from Fab-1, including process target and equipment type
  - Detailed process flow of 0.25um 6T SRAM (ISSI customer) from Fab-1, Fab-2 and T Fab-5, including process target and equipment type.
  - Detailed process flow of 0.25um Logic (TSMC) from Fab-1 and Fab-2, including proc target and equipment type
  - Detailed process flow of 0.22um Logic (TSMC) from Fab-1 and Fab-2, including proc target and equipment type
  - Detailed process flow of 0.18um Logic (TSMC) from Fab-2, including process target equipment type

The priority is following the order.

- **Training**

Since we are starting to hire some Shanghanese technicians and engineers to send to our oversee Operation, we need to think about the training we have to give them.

Can you pull-out from WSMC and TSMC the training plan for the new hired technicians an engineers? Also, if you can pull-out some of their training material, both in Chinese and Eng will be very helpful.

Sorry for the long list, but we need a lot of material to set-up the new operation.

See you soon,

Best Regards, Marco

B7

Exhibit B

US006274514B1

(12) **United States Patent**
Jang et al.

(10) **Patent No.: US 6,274,514 B1**
(45) **Date of Patent: Aug. 14, 2001**

(54) **HDP-CVD METHOD FOR FORMING PASSIVATION LAYERS WITH ENHANCED ADHESION**

(75) Inventors: **Syun-Ming Jang**, Hsin-Chu; **Chu-Yun Fu**, Taipei, both of (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company**, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/336,807**

(22) Filed: **Jun. 21, 1999**

(51) **Int. Cl.**[7] **H01L 21/31**; H01L 21/469
(52) **U.S. Cl.** **438/778**; 438/798; 438/127
(58) **Field of Search** 438/778, 666, 438/667, 668, 672, 673, 688, 680, 622, 127, 124, 122, 623–626

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,494,854 2/1996 Jain .
5,756,380 5/1998 Berg 438/126
5,759,906 * 6/1998 Lou 438/623
5,804,259 9/1998 Robles 427/577
5,807,768 * 9/1998 Shin 438/127
6,046,106 * 4/2000 Tran et al. 438/660
6,087,278 * 7/2000 Kim et al. 438/978

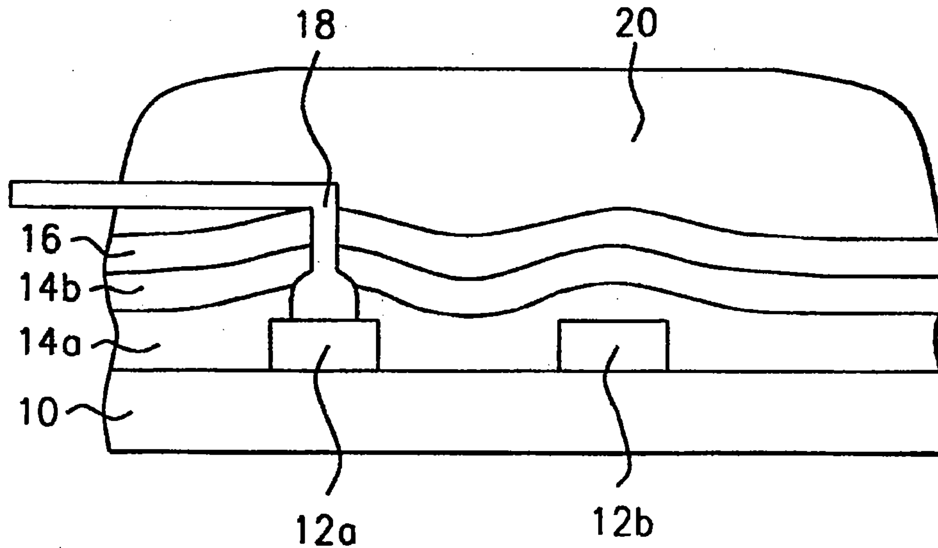
* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Dung A Le
(74) *Attorney, Agent, or Firm*—George O. Saile; Stephen B. Ackerman; Alek P. Szecsy

(57) **ABSTRACT**

A method for forming upon a substrate employed within a microelectronics fabrication a dielectric passivating layer with attenuated delamination and improved adhesion to subsequent passivating and encapsulating materials. There is first provided a substrate employed within a microelectronics fabrication. There is then formed upon the substrate a patterned microelectronics layer. There is then formed over the substrate a silicon containing dielectric layer employing high density plasma chemical vapor deposition (HDP-CVD) in two steps, wherein the conditions of the HDP-CVD process are optimized during the second step to provide a final layer portion with a greater degree of surface topography. Subsequently there are formed over the substrate an additional passivation layer with attenuated delamination and an organic polymer overcoat layer with improved adhesion.

13 Claims, 1 Drawing Sheet



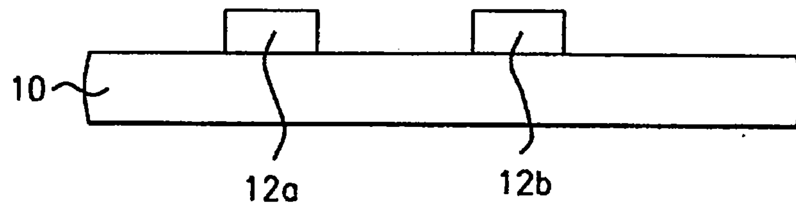


FIG. 1

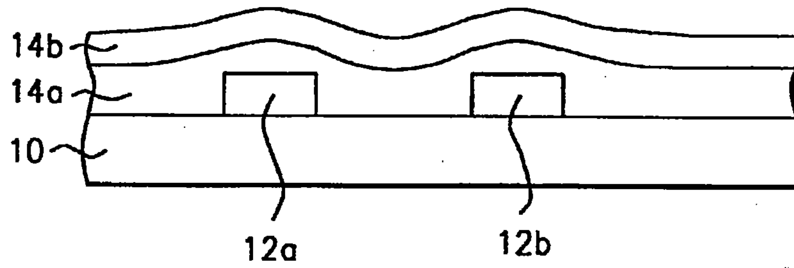


FIG. 2

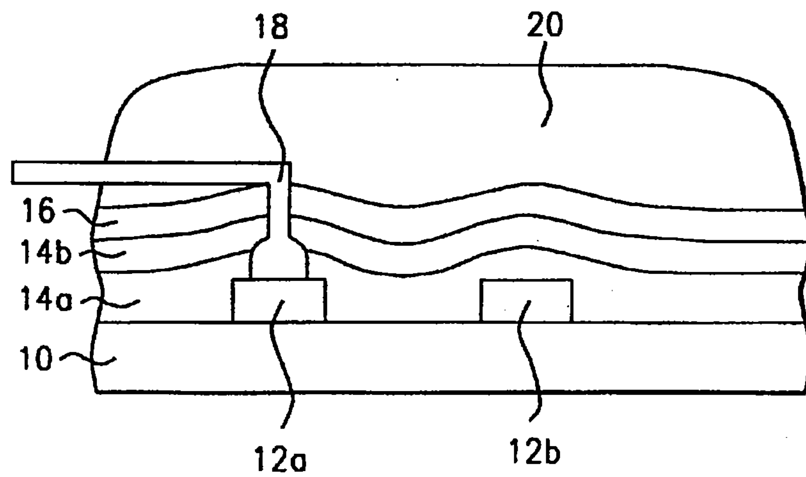


FIG. 3

HDP-CVD METHOD FOR FORMING PASSIVATION LAYERS WITH ENHANCED ADHESION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to the field of dielectric layers employed within microelectronics fabrications. More particularly, the invention relates to the field of delamination resistant dielectric layers employed for passivation of microelectronics fabrications.

2. Description of the Related Art.

As the dimensions of microelectronics fabrications have decreased, the sensitivity of such devices to environmental factors has required that the methods for passivation and protection of microelectronics fabrications be improved. Microelectronics fabrications are passivated and protected primarily by insuring that the surfaces of the fabrications be covered and sealed with impervious coatings of chemically and physically stable materials, and secondarily by placing the completed fabrication with its attendant electrical leads and connections within another protective enclosure or "package" so that the device may be handled and employed as designed with reasonable security from any potentially harmful environment. To insure adequate protection, the protective structures must be inherently free from porosity and their fabrication must insure freedom from cracks or defects at joints, interfaces and seams.

The primary passivation of microelectronics fabrications, particularly those employing semiconductor materials which are especially sensitive to extremely small chemical or physical changes at their surfaces, is generally achieved by forming individual or composite surface layers of silicon containing dielectric materials such as silicon oxide or silicon nitride because of the excellent physical and chemical stability of these materials and their relative ease of formation and methods of shaping. The secondary protective methods, or packaging, of microelectronics fabrications generally employ thermoplastic or thermosetting organic polymer materials molded as overcoating layers around the microelectronics fabrication with its attendant attached leads and connections. This method is particularly widely employed in situations where manufacturing cost is an important factor and environmental conditions for use of the device are not very severe.

Although satisfactory methods of passivation with silicon containing dielectric materials and packaging with molded organic polymer materials are available for microelectronics fabrications, these methods of protecting microelectronics fabrications are not without problems. In particular, composite silicon containing dielectric layers and molded organic polymer materials formed around devices coated with silicon containing passivation layers often experience difficulties due to poor adhesion of the molded organic polymer material to surfaces typical of silicon containing dielectric layers, as well as delamination between the composite layers.

It is towards the goal of providing enhanced adhesion of protective layers and coatings to microelectronics fabrications that the present invention is generally and more specifically directed.

Various methods have been disclosed for forming passivation layers and protective packaging enclosures upon microelectronics fabrications.

For example, Jain, in U.S. Pat. No. 5,494,854, discloses a method for forming a planarized dielectric passivation layer upon a patterned layer semiconductor microelectronics fabrication. The method first forms a gap filling silicon oxide dielectric layer by high density plasma chemical vapor deposition, followed by a second silicon oxide dielectric layer formed by plasma enhanced chemical vapor deposition and subsequent chemical mechanical polish (CMP) planarization.

Further, Berg et al., in U.S. Pat. No. 5,756,380, disclose a method for forming a moisture resistant microelectronics fabrication employing an organic substrate which is resistant to delamination or cracking at interfaces. The method employs organic polymer materials for attachment of the microelectronics fabrication to the substrate and for overall encapsulation.

Still further, Lou, in U.S. Pat. No. 5,759,906, discloses a method for forming a planarized inter-level metal dielectric (IMD) layer with via contact holes on integrated circuit microelectronics fabrications. The method employs combinations of dielectric layers formed employing plasma enhanced chemical vapor deposition (PECVD) and low dielectric constant dielectric layers formed from spin-on-glass (SOG) dielectric materials as well as chemical mechanical polish (CMP) planarization to realize the planar inter-level metal dielectric (IMD) layer. Multiple baking steps between fabrication of layers is employed to minimize via contact hole poisoning.

Yet still further, Robles, in U.S. Pat. No. 5,804,259, discloses a method for forming a multi-layer low dielectric constant dielectric layer on a substrate. The method employs forming a first layer of carbonaceous diamond-like dielectric material followed by layers of organic polymer dielectric materials such as poly-p-xylylene (Parylene) to form a composite low dielectric constant dielectric layer.

Finally, Shin, in U.S. Pat. No. 5,807,768, discloses a method for forming a package of molded epoxy resin to encapsulate a semiconductor integrated circuit microelectronics fabrication and integral heat sink. The molded package is fabricated in two parts, the first being of greater bonding strength than the second, to afford greater resistance to delamination at the interface between the first molded part and the integrated circuit microelectronics fabrication integral heat sink combination.

Desirable in the art of microelectronics fabrication are additional methods and materials for forming passivation layers and molded organic polymer package structures with improved resistance to delamination or other structural failure modes.

It is towards these goals that the present invention is generally and specifically directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method for forming upon a substrate employed within a microelectronics fabrication a dielectric layer with improved adhesion to encapsulating materials subsequently formed thereupon.

A second object of the present invention is to provide a method in accord with the first object of the present invention, where there is attenuated delamination of dielectric passivation layers formed over dielectric layers formed upon a substrate employed within an integrated circuit microelectronics fabrication and improved adhesion to organic polymer encapsulating materials formed thereover.

A third object of the present invention is to provide a method in accord with the first object of the present inven-

tion and/or the second object of the present invention, where the method is readily commercially implemented.

In accord with the objects of the present invention, there is provided a method for forming upon a substrate employed within a microelectronics fabrication a dielectric passivation layer with attenuated delamination from underlying dielectric layers and with improved adhesion to encapsulating materials subsequently formed thereupon. To practice the method of the present invention, there is first provided a substrate employed within a microelectronics fabrication. There is then formed upon the substrate a silicon containing dielectric layer employing the method of high density plasma chemical vapor deposition (HDP-CVD). There is then formed over the silicon containing dielectric passivation layer an additional passivation layer and an organic polymer material overcoat layer formed over and around the microelectronics fabrication as a protective package.

The present invention provides a method for forming a dielectric passivation layer over, and exhibiting attenuated delamination from, a silicon containing dielectric layer formed upon a substrate employed within a microelectronics fabrication, and for forming a molded organic polymer overcoat over the substrate with improved adhesion to the underlying passivation layer.

The method of the present invention may be advantageously employed within microelectronics fabrications including but not limited to integrated circuit microelectronics fabrications, charge coupled device microelectronics fabrications, solar cell microelectronics fabrications, light emitting diode microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

The method of the present invention employs materials and methods as are known in the art of microelectronics fabrications, but in a novel order, sequence and range of parameters. Hence the method of the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

FIG. 1, FIG. 2 and FIG. 3 are directed towards a general embodiment of the present invention. Shown in FIG. 1 to FIG. 3 is a series of schematic cross-sectional diagrams illustrating the results of forming upon a substrate employed within a microelectronics fabrication a dielectric passivation layer with attenuated delamination from layers subsequently deposited thereon. and to enhanced adhesion to protective organic polymer overcoat layers formed thereupon.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a method for forming upon a dielectric layer formed over a substrate employed within a microelectronics fabrication a dielectric passivation layer with attenuated delamination from layers formed thereunder, and improved adhesion to organic polymer overcoat layers fried thereover.

Referring now to FIG. 1 to FIG. 3, there is shown a series of schematic cross-sectional diagrams illustrating the results of forming upon a substrate employed within a microelectronics fabrication a dielectric passivation layer in accord with a general embodiment of the present invention. FIG. 1 is a schematic cross-sectional diagram of a microelectronics fabrication at an early stage in its fabrication.

Shown in FIG. 1 is a substrate **10** upon which is formed a series of patterned microelectronics layers **12*a*** and **12*b***. The substrate **10** may be the substrate itself employed within the microelectronics fabrication, or alternatively, the substrate **10** may be the substrate employed within the microelectronics fabrication with any of several microelectronics layers formed thereupon. The substrate **10** may be selected from the group including but not limited to microelectronics conductor substrates, microelectronics semiconductor substrates and microelectronics dielectric substrates employed within microelectronics fabrications including but not limited to integrated circuit microelectronics fabrications, charge coupled device microelectronics fabrications, solar cell microelectronics fabrications, light emitting diode microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

With respect to the series of patterned microelectronics layers **12*a*** and **12*b***, the series of patterned microelectronics layers **12*a*** and **12*b*** may be formed from microelectronics materials including but not limited to microelectronics conductor materials, microelectronics semiconductor materials and microelectronics dielectric materials. The microelectronics materials may be deposited employing methods as are known in the art of microelectronics fabrication including but not limited to thermal vacuum evaporation methods, electron beam evaporation methods, chemical vapor deposition (CVD) methods, physical vapor deposition (PVD) sputtering methods and reactive sputtering methods. Patterning of microelectronics layers may be accomplished employing photolithographic methods and materials as are known in the art of microelectronics fabrication.

Referring now more particularly to FIG. 2, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in FIG. 1. Shown in FIG. 2 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in FIG. 1, but where there has been formed over and upon the substrate **10** a silicon containing dielectric layer **14*a*** and **14*b*** formed employing the method of high density plasma chemical vapor deposition (HDP-CVD).

With respect to the silicon containing dielectric layer **14*a*** and **14*b*** shown in FIG. 2, the silicon containing dielectric layer **14*a*** and **14*b*** is formed employing high density plasma chemical vapor deposition (HDP-CVD) wherein the deposition is done in two steps: the first portion of the dielectric layer **14*a*** is deposited at a first lower deposition:sputter ratio to provide better gap filling, and the latter portion of the dielectric layer **14*b*** is formed at a second higher deposition-:sputter ratio to provide a topographically rougher surface of the silicon containing glass dielectric passivation layer **14*b***. Preferably, the high density plasma chemical vapor deposition (HDP-CVD) method employs the following process for the first portion **14*a***: (1) gas flow rates of argon of from about 110 to about 130 standard cubic centimeters per minute (sccm), oxygen from about 90 to about 110 standard cubic centimeters per minute (sccm), and silage (SiH_4) of from about 50 to about 60 standard cubic centimeters per minute (sccm); (2) total pressure of from about 4 to about 6 mtorr; (3) temperature of from about 400 to about 430 degrees centigrade; (4) source power of from about 4000 to about 5000 watts; (5) bias power of from about 2500 to

about 3500 watts. For the second portion *14b*, the HDP-CVD method preferably employs the following process; (1) gas flow rates of argon of from about 110 to about 130 standard cubic centimeters per minute (sccm), oxygen of from about 180 to about 200 standard cubic centimeters per minute (sccm) and silane (SiH_4) of from about 100 to about 110 standard cubic centimeters per minute (sccm); (2) total pressure of from about 7 to about 10 mtorr; (3) temperature from about 400 to about 430 degrees centigrade; (4) source power from about 4000 to about 5000 watts; (5) bias power from about 2500 to about 3500 watts.The silicon containing glass dielectric layer *14a* and *14b* is preferably formed to a total thickness of from about 8000 to about 12,000 angstroms.

Referring now more particularly to FIG. 3, there is shown a schematic cross sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in FIG. 2. Shown in FIG. 3 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in FIG. 2, but where there has been formed upon the dielectric passivation layer **14b** an additional dielectric passivation layer **16**. A wire electrical lead **18** is bonded to a conductive portion of the patterned microelectronics layer **12a**. Formed around the entire microelectronics fabrication is a molded organic polymer encapsulating structure **20**.

With respect to the second dielectric passivation layer **16** shown in FIG. 3, the additional dielectric passivation layer **16** may be formed from silicon containing dielectric materials including but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials employing methods known in the art of microelectronics fabrication including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods, sub-atmospheric pressure thermal chemical vapor deposition (SACVD) methods, physical vapor deposition (PVD) sputtering methods and reactive sputtering methods. Although not shown in FIG. 3, the additional passivation layer comprising the dielectric passivation layer **16** may be formed from more than one additional dielectric layer. Preferably the additional dielectric passivation layer **16** is formed of silicon nitride dielectric material employing a plasma enhanced chemical vapor deposition (PECVD) method. Preferably the additional dielectric passivation layer **16** is formed to a thickness of from about 5000 to about 10,000 angstroms.

With respect to the wire lead electrical connection **18** shown in FIG. 3, the wire lead electrical connection **18** is fabricated employing materials and methods well known in the art of microelectronics fabrication.

With respect to the molded organic polymer overcoat layer **20** shown in FIG. 3, the molded organic polymer overcoat layer **20** is formed employing materials and methods which are known in the art of microelectronics fabrication. Preferably, the molded organic polymer overcoat layer is formed from an epoxy resin formulation suited to injection molding.

The beneficial effect of the present invention is observed with respect to the improvement of adhesion of molded organic polymer packaging structures to silicon containing dielectric materials formed into layers employing the method of high density plasma chemical vapor deposition (HDP-CVD), wherein the dielectric layers formed in this fashion possess excellent physical and chemical properties with respect stability and freedom from undesirable impurities. These properties render these dielectric materials desirable as dielectric passivation layers employed within microelectronics fabrications, but such dielectric materials tend to have smooth planarized surfaces such that adhesion to other materials formed thereon may not be adequate, and delamination between dielectric layers may occur. Additionally, poor adhesion of the organic polymer overcoat layer to the underlying passivation layer may also occur. The greater amount of surface topography which occurs during formation of silicon containing dielectric layers at high deposition:sputter rate ratios during high plasma density chemical vapor deposition (HDP-CVD) is therefore of beneficial effect to attenuate delamination and to improve adhesion of overlying layers. Conversely, the formation of silicon containing glass dielectric layers at low deposition: sputter rate ratios provides dielectric layers with better gap filling capability as is desirable for passivation of microelectronics fabrications.

As is understood by a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to materials, structures and dimensions through which is provided the preferred embodiments of the present invention while still providing embodiments which are within the spirit and scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A method for passivating a microelectronics fabrication comprising:
   - providing a substrate;
   - forming upon the substrate a patterned microelectronics layer;
   - forming over the patterned microelectronics layer a first portion of a first dielectric layer formed employing a high density plasma chemical vapor deposition (HDP-CVD) method employing a first deposition:sputtering ratio;
   - forming upon the first portion of the first dielectric layer a second and completing portion of the first dielectric layer formed employing a second high density plasma chemical vapor deposition (HDP-CVD) method employing a second deposition:sputtering ratio;
   - forming over the first dielectric layer one or more additional silicon containing dielectric passivation layer; and
   - forming an overcoating molded organic polymer layer over the passivation layer and substrate.

2. The method of claim 1 wherein the substrate is employed within a microelectronics fabrication selected from the group consisting of:
   - integrated circuit microelectronics fabrications;
   - charge coupled device microelectronics fabrications;
   - solar cell microelectronics fabrications;
   - radiation emitting diode microelectronics fabrications;
   - ceramics substrate microelectronics fabrications; and
   - flat panel display microelectronics fabrications.

3. The method of claim 1 wherein the patterned microelectronics layers are selected from the group of microelectronics materials comprising:
   - microelectronics conductor materials;
   - microelectronics semiconductor materials; and
   - microelectronics dielectric materials.

4. The method of claim 1 wherein the first dielectric layer is formed by a two step high density plasma chemical vapor deposition (HDP-CVD) method comprising:

a first deposition step of a silicon containing glass dielectric material at a first lower deposition:sputtering ratio selected to optimize the gap filling quality of the silicon containing glass dielectric layer portion; and

a second deposition step of a silicon containing glass dielectric material at a second higher deposition:sputtering ratio selected to optimize the surface topography of the silicon containing glass dielectric layer portion for subsequent attenuated delamination of additional overlying passivation layers and improved adhesion to an overcoating layer.

5. The method of claim 1 wherein the additional silicon containing dielectric passivation layer is formed employing plasma enhanced chemical vapor deposition (PECVD).

6. The method of claim 5 wherein the silicon containing dielectric material is selected from the group consisting of:

silicon nitride;

silicon oxynitride; and

silicon oxide.

7. The method of claim 1 wherein the overcoating molded organic polymer layer is formed from an epoxy resin formulation suited for injection molding.

8. A method for passivating an integrated circuit microelectronics fabrication comprising:

providing a semiconductor substrate having formed therein integrated circuit components;

forming upon the semiconductor substrate a patterned microelectronics layer;

forming over the patterned microelectronics layer a first portion of a first silicon containing dielectric layer employing a high density plasma chemical vapor deposition (HDP-CVD) method employing a first lower deposition:sputter ratio optimized to fill a series of gaps defined by a series of patterns within the patterned microelectronics layer;

forming upon the first portion of the first silicon containing dielectric layer a second and completing portion of the first silicon containing dielectric layer employing a second higher deposition:sputtering ratio optimized to increase surface topography;

forming a silicon nitride dielectric passivation layer over the first silicon containing dielectric layer with attenuated delamination of the underlying portions of the first silicon containing dielectric layer;

attaching interconnection leads to the integrated circuit components; and

forming an overcoating molded organic polymer layer over the silicon nitride passivation layer and semiconductor substrate with improved adhesion.

9. The method of claim 8 wherein the semiconductor substrate is a silicon semiconductor substrate.

10. The method of claim 8 wherein the first silicon containing dielectric layer is a silicon oxide dielectric layer.

11. The method of claim 8 wherein the passivation layer is a silicon nitride layer formed employing plasma enhanced (PECVD) chemical vapor deposition.

12. The method of claim 8 wherein the overcoating molded organic polymer layer is formed from epoxy resin formulated for injection molding.

13. The method of claim 8 wherein the interconnection leads are bonded to contact regions formed on the semiconductor substrate surface prior to molding the organic polymer overcoat upon and around the substrate.

* * * * *

Exhibit C

United States Patent [19]

Shiue et al.

[11] **Patent Number: 5,923,088**

[45] **Date of Patent: Jul. 13, 1999**

[54] **BOND PAD STRUCTURE FOR THE VIA PLUG PROCESS**

[75] Inventors: **Ruey-Yun Shiue; Wen-Teng Wu; Pi-Chen Shieh; Chin-Kai Liu**, all of Hsin-Chu, Taiwan

[73] Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu, Taiwan

[21] Appl. No.: **08/929,953**

[22] Filed: **Sep. 15, 1997**

Related U.S. Application Data

[62] Division of application No. 08/703,918, Aug. 22, 1996, Pat. No. 5,700,735.

[51] **Int. Cl.**[6] **H01L 23/522**

[52] **U.S. Cl.** **257/758**; 257/774; 257/781; 257/786

[58] **Field of Search** 257/761, 781, 257/786, 780, 758

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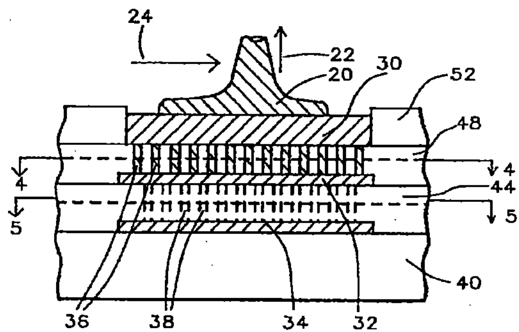
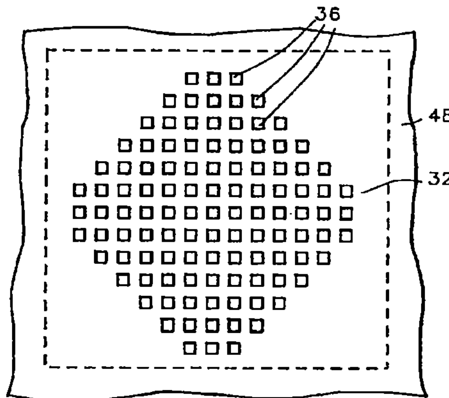
Primary Examiner—David B. Hardy
Attorney, Agent, or Firm—George O. Saile; Stephen B. Ackerman; Larry J. Prescott

[57] **ABSTRACT**

A bond pad structure and method of forming the bond pad structure which provides for reliable interconnections between the bond pad structure and the next level of circuit integration. The bond pad structure uses three metal pads separated by layers of dielectric. Via plugs are formed between the first and second metal pads and between the second and third metal pads. The via plugs are formed in a diamond shape with respect to the metal pads. The metal pads are squares with the same orientation. The periphery of the via plugs forms a square rotated 45° with respect to the square metal pads.

9 Claims, 4 Drawing Sheets





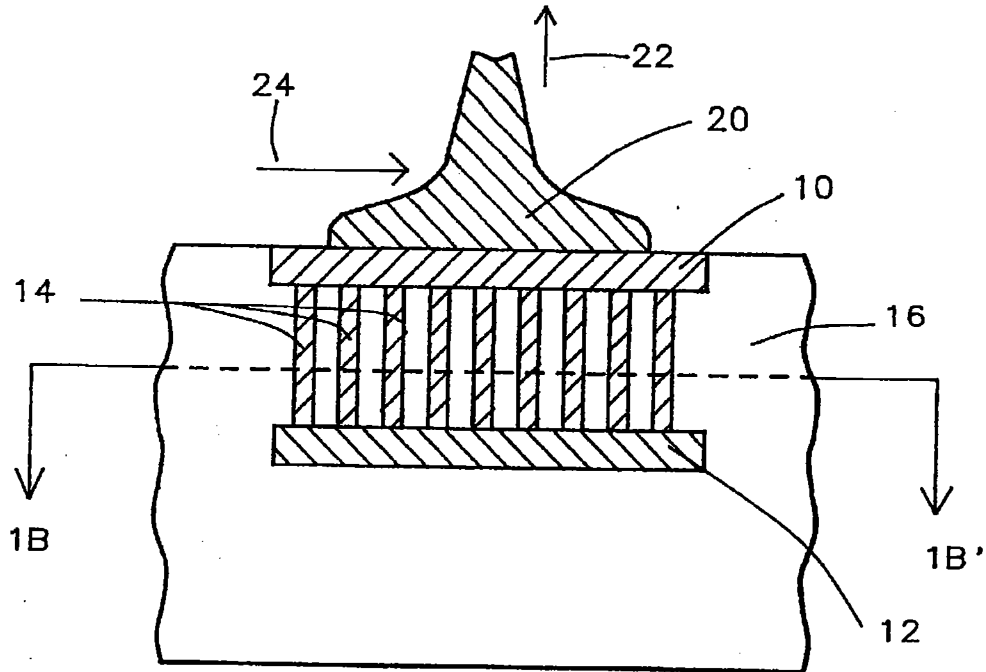


FIG. 1A – Prior Art

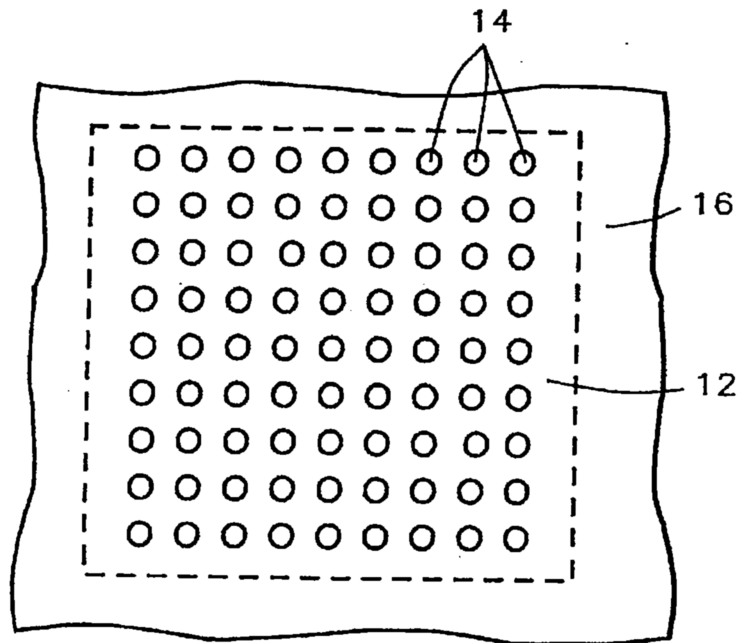


FIG. 1B – Prior Art

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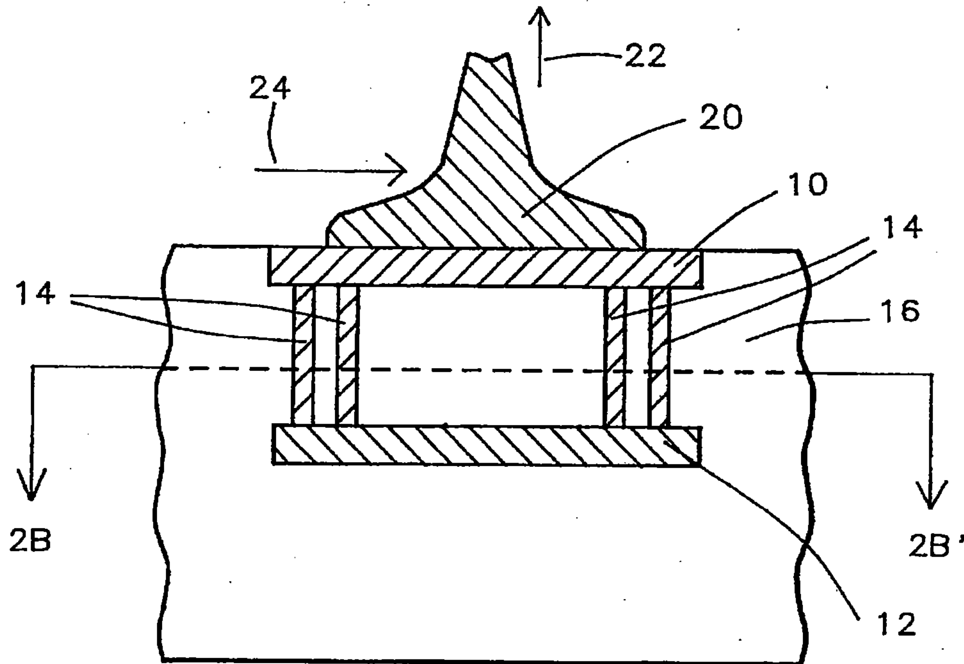

FIG. 2A – Prior Art

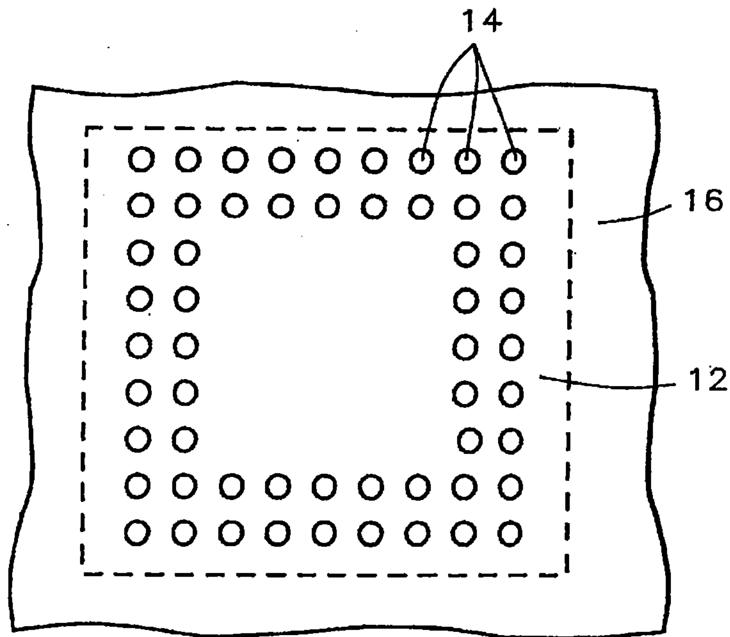

FIG. 2B – Prior Art

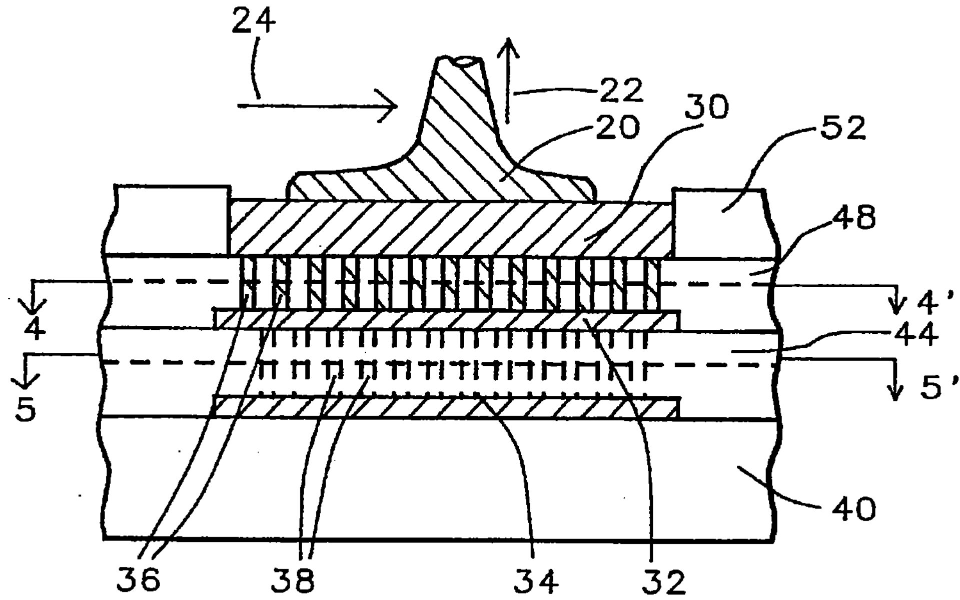

FIG. 3

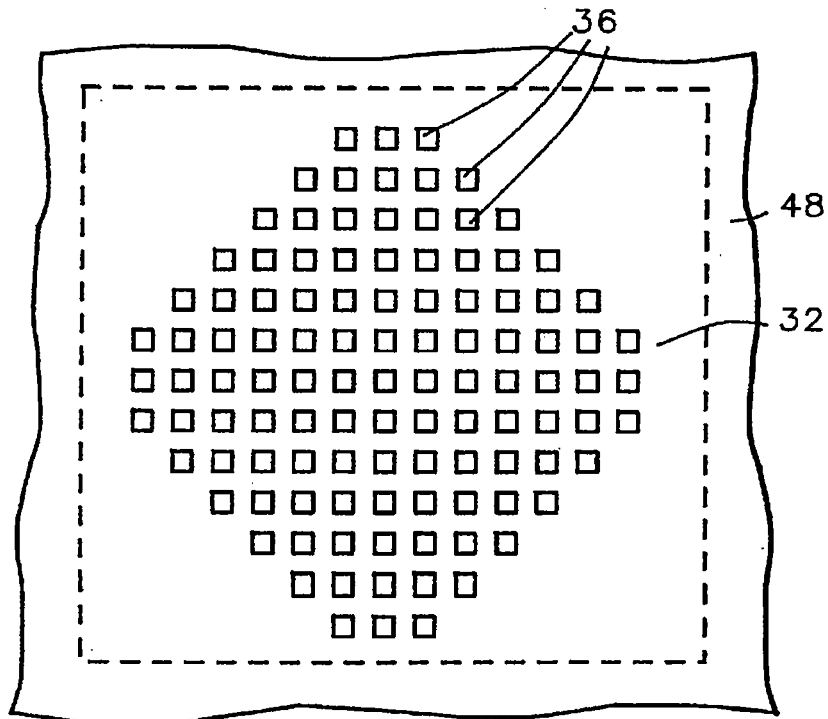

FIG. 4

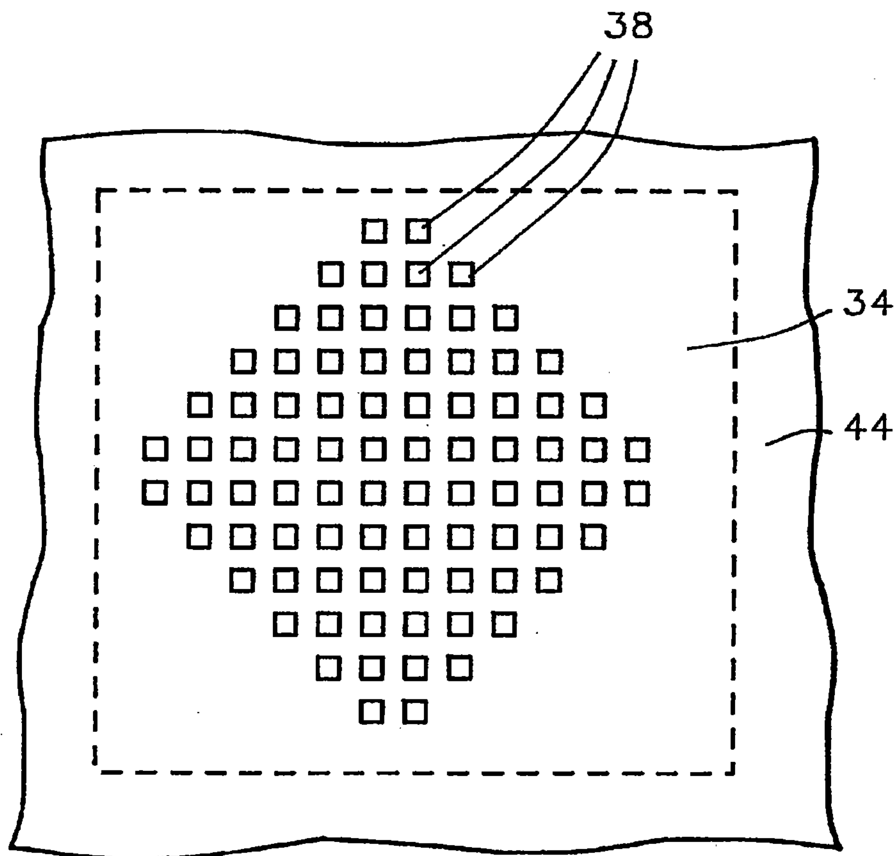

FIG. 5

BOND PAD STRUCTURE FOR THE VIA PLUG PROCESS

This is a division of patent application Ser. No. 08/703, 918, filing date Aug. 22, 1996, A Novel Bond Pad Structure and Method Of Forming The Structure For The Via Plug Process, assigned to the same assignee as the present invention, now U.S. Pat. No. 5,700,735.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to the structure of bond pads using the via plug process and more specifically to bond pads using three metal pad layers with via plugs between the first and second metal pad layers and between the second and third metal pad layers.

(2) Description of the Related Art

When an integrated circuit element has been completed electrical connections must be made to the next level of integration after the integrated circuit element. Bond pads provide a location for bonding wires or other connectors for this purpose. It is important that the bond pad structure be reliable and provide a reliable bond or the integrated circuit element will become useless.

A bond pad structure is shown in U.S. Pat. No. 5,266,522 to DiGiacomo et al. using metallurgy chosen to minimize corrosion and stress in the bond. U.S. Pat. No. 5,403,777 to Bryant et al. describes a bond pad using a barrier layer followed by two conducting layers to form a bond pad with good adhesion.

This invention provides a bond pad using three layers of metal pads with via plugs between the layers and is different than the bond pads described by DiGiacomo et al. or Bryant et al.

SUMMARY OF THE INVENTION

In circuit packages for integrated circuit elements and the like bond pads are often used to make electrical connections between the circuit package and the next level of integration. Interconnection wires are bonded to the bond pads and to the next level of integration.

Reliability of these bond pads is of critical importance and the wire to bond pad connection should withstand critical values of tensile and shear forces without failure. In order to test bond pads wires are bonded to a sample and subjected to tensile strength and shear strength testing. During such tensile strength and shear strength testing bond pad peeling and cracking must be minimized along with obtaining adequate tensile strength and shear strength values.

It is a principle objective of this invention to provide a bond pad structure which will provide adequate tensile strength and shear strength for a bond formed on the bond pad structure as well as reducing the frequency of bond pad peeling and cracking.

It is a further objective of this invention to provide a method of forming a bond pad structure which will provide adequate tensile strength and shear strength for a bond formed on the bond pad structure as well as reducing the frequency of bond pad peeling and cracking.

These objectives are achieved by forming a bond pad structure having two layers of via plugs formed between three metal layers. The via plugs are arranged in a diamond pattern and neither layer of via plugs is directly above the other. One of the three metal layers forms the bonding surface.

Examples of conventional bond pad structures are shown in FIGS. 1A–2B. FIG. 1A shows a cross section of the a bond pad showing a first metal pad **10** formed of a material such as AlCu/TiN and a second metal pad **12** formed of a material such as AlCu/TiN formed in a dielectric material **16** such as silicon dioxide formed using plasma enhanced deposition of tetraethyl orthosilicate. Via plugs **14** formed of a material such as tungsten are formed between the first metal pad **10** and the second metal pad **12**. A test fixture **20** is shown bonded to the first metal pad **10**. In testing the bond pad a tensile force **22** or a shear force **24** is applied to the test fixture **20**.

FIG. 1B shows a plan view of the bond pad along the line 1B-1B' in FIG. 1A. The via plugs **14** are shown in a square array having the same orientation as the first metal pad **10** and the second metal pad **12**. The second metal pad **12** is shown by a dashed line in FIG. 1B since the second metal pad is covered by the dielectric material **16**. For the bond pad structure of FIGS. 1A and 1B the first metal pad and the second metal pad are each about 100 microns square and there are 81 via plugs each having a diameter of about 0.6 microns. These pads fail with a large amount of pad peeling.

FIGS. 2A and 2B show another example of a conventional bond pad structure. This bond pad structure is the same as the previous example except there are 56 via plugs **14** wherein these via plugs lie on two squares. FIG. 2A shows a cross section of the bond pad structure showing the via plugs **14** formed in a ceramic material **16** between a first metal pad **10** and a second metal pad **12**. A test fixture **20** is shown bonded to the first metal pad **10**. In testing the bond pad a tensile force **22** or a shear force **24** is applied to the test fixture **20**.

FIG. 2B shows a plan view of the bond pad along the line 2B-2B' in FIG. 2A. The via plugs **14** are shown in a square array having the same orientation as the first metal pad **10** and the second metal pad **12**. The second metal pad **12** is shown by a dashed line in FIG. 2B since the second metal pad is covered by the dielectric material **16**. For the bond pad structure of FIGS. 2A and 2B the first metal pad and the second metal pad are each about 100 microns square and there are 56 via plugs each having a diameter of about 0.6 microns. These pads fail with a large amount of pad peeling.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows a cross section view of a prior art bond pad.

FIG. 1B shows a plan view of a prior art bond pad along the line 1B-1B' of FIG. 1A.

FIG. 2A shows a cross section view of a prior art bond pad.

FIG. 2B shows a plan view of a prior art bond pad along the line 2B-2B' of FIG. 2A.

FIG. 3 shows a cross section view of the bond pad of this invention.

FIG. 4 shows a plan view of the bond pad of this invention along the line 4-4' of FIG. 3.

FIG. 5 shows a plan view of the bond pad of this invention along the line 5-5' of FIG. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to FIGS. 3–5, there is shown an embodiment of the bond pad structure of this invention. FIG. 3 shows a cross section view of the bond pad structure of this embodiment. As shown in FIG. 3 a first metal pad **34**, a second

metal pad 32, and a third metal pad 30 are formed in a dielectric. A first number, between about 70 and 110, of first via plugs 38 are formed between the first metal pad 34 and the second metal pad 32. A second number, between about 85 and 135, of second via plugs 36 are formed between the second metal pad 32 and the third metal pad 30. The first number of first via plugs 38 are shown as dashed lines in FIG. 3 since the first via plugs are not in the same plane as the second via plugs 36 and are covered by dielectric material 44.

The third metal pad 30 is formed from a material such as AlCu/TiN, has a thickness of between about 6400 and 10,000 Angstroms, a length of between about 80 and 120 microns, and a width of between about 80 and 120 microns. The second metal pad 32 is formed from a material such as AlCu/TiN, has a thickness of between about 4000 and 7000 Angstroms, a length of between about 80 and 120 microns, and a width of between about 80 and 120 microns. The first metal pad 34 is formed from a material such as AlCu/TiN, has a thickness of between about 4000 and 7000 Angstroms, a length of between about 80 and 120 microns, and a width of between about 80 and 120 microns. The second via plugs 36 are formed of a material such as tungsten, have a square cross section of between about 0.4 and 0.8 microns by between about 0.4 and 0.8 microns, and have a length of between about 0.4 and 0.8 microns. The first via plugs 38 are formed of a material such as tungsten, have a square cross section of between about 0.4 and 0.8 microns by between about 0.4 and 0.8 microns, and have a length of between about 0.4 and 0.8 microns.

The first metal pad 34 is formed on a first dielectric layer 40. A second dielectric layer 44 is formed over the first metal pad 34 between the first metal pad 34 and the second metal pad 32 and has a thickness of between about 6000 and 10,000 Angstroms. The second metal pad 32 is formed on the second dielectric layer 44. The first via plugs 38 are formed in the second dielectric layer 44 and make contact with the first metal pad 34 and the second metal pad 32. A third dielectric layer 48 having a thickness of between about 6000 and 10,000 Angstroms is formed between the second metal pad 32 and the third metal pad 30. The third metal pad 30 is formed on the third dielectric layer 48. A fourth dielectric layer 52 having a thickness of between about 8000 and 12,000 Angstroms is formed on the third dielectric layer 48 after the formation of the third metal pad 30 so that the fourth dielectric layer surrounds and overlaps the edges of the third metal pad 30. The second via plugs 36 are formed in the third dielectric layer 48 and make contact with the second metal pad 32 and the third metal pad 30.

FIG. 3 shows a test fixture 20 bonded to the first metal pad 30. Either tensile forces 22 or shear forces 24 can be applied to the test fixture 20. The first, second, third, and fourth dielectric layers are formed of a material such as silicon dioxide formed using plasma enhanced deposition of tetraethyl orthosilicate.

FIG. 4 shows a plan view of the bond pad structure along the line 4-4' of FIG. 3. FIG. 4 shows the second via plugs 36 formed in the third dielectric layer 48. The second metal pad 32 is shown using a dashed line since it is covered by the third dielectric layer 48. The second via plugs 36 are square having a width of between about 0.6 and 0.8 microns. The second via plugs 36 are arranged in a diamond shape when compared to the second metal pad 32. The periphery of the first via plugs forms a square rotated 45° with respect to the second metal pad 32. The first metal pad, second metal pad, and third metal pad are squares having the same orientation.

FIG. 5 shows a plan view of the bond pad structure along the line 5-5' of FIG. 3. FIG. 5 shows the first via plugs 38 formed in the second dielectric layer 44. The first metal pad 34 is shown using a dashed line since it is covered by the second dielectric layer 44. The first via plugs 38 are square having a width of between about 0.6 and 0.8 microns. The first via plugs 38 are arranged as a diamond shape when compared to the first metal pad 34. The periphery of the first via plugs forms a square rotated 45° with respect to the first metal pad 34. The first metal pad, second metal pad, and third metal pad are squares having the same orientation. The second via plugs 36 are not located directly above the first via plugs 38, see FIG. 3, but are located directly over the spaces between the first via plugs 38.

This arrangement of three metal pads, first via plug array, and second via plug array provides improved strength and reliability for the bond pad. As shown in FIG. 3, a test fixture 20 can be bonded to the third metal pad 30. Either tensile forces 22 or shear forces 24 can be applied to the test fixture 20. For the bond pad described in this embodiment 0.01% of the bond pads fail with tensile forces up to 5 grams and 0.1% of the bond pads fail with shear forces up to 35 grams. Almost none of these failures are due to bond pad peeling.

Refer now to FIG. 3, there is shown an embodiment of a method of forming the bond pad structure of this invention. A first dielectric layer 40 having a thickness of between about 8000 and 12,000 Angstroms is formed of a material such as boron/phosphorus doped silicon dioxide using deposition of tetraethyl orthosilicate. A first metal pad 34, formed of a material such as AlCu/TiN having a length of between about 80 and 120 microns, a width of between about 80 and 120 microns, and a thickness of between about 4000 and 7000 Angstroms, is formed on the first dielectric layer 40. A second dielectric layer 44 having a thickness of between about 8000 and 10,000 Angstroms is formed of a material such as silicon dioxide using plasma enhanced deposition of tetraethyl orthosilicate on the first dielectric layer 40 covering the first metal pad 34. Openings for the first via plugs 38, having a square cross section of between about 0.4 and 0.8 microns by between about 0.4 and 0.8 microns, are formed in the second dielectric layer 44 and filled with a metal such as tungsten thereby forming the first via plugs 38.

A second metal pad 32, formed of a material such as AlCu/TiN having a length of between about 80 and 120 microns, a width of between about 80 and 120 microns, and a thickness of between about 4000 and 7000 Angstroms, is formed on the second dielectric layer 44 forming contact with the first via plugs 38. A third dielectric layer 48 having a thickness of between about 6000 and 10,000 Angstroms is formed of a material such as silicon dioxide using plasma enhanced deposition of tetraethyl orthosilicate on the second dielectric layer 44 covering the second metal pad 32. Openings for the second via plugs 36, having a square cross section of between about 0.4 and 0.8 microns by between about 0.4 and 0.8 microns, are formed in the third dielectric layer 48 and filled with a metal such as tungsten thereby forming the second via plugs 36.

A third metal pad 30, formed of a material such as AlCu/TiN having a length of between about 80 and 120 microns, a width of between about 80 and 120 microns, and a thickness of between about 7000 and 10,000 Angstroms, is formed on the third dielectric layer 48 forming contact with the second via plugs 36. A fourth dielectric layer 52 having a thickness of between about 8000 and 12,000 Angstroms is formed of a material such as silicon dioxide using plasma enhanced deposition of tetraethyl orthosilicate on the third dielectric layer 48 covering the third metal pad 30. Most of that part of the fourth dielectric layer directly over the third metal pad 30 is then etched away leaving some of the fourth dielectric layer 52 overlapping the edges of the third metal pad 30.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A bond pad structure, comprising:

a first dielectric layer;

a square first metal pad formed on said first dielectric layer;

a second dielectric layer formed over said first metal pad;

a square second metal pad formed over said second dielectric layer wherein said second metal pad is directly above said first metal pad and has the same orientation as said first metal pad;

a third dielectric layer formed over said second metal pad;

a square third metal pad formed over said third dielectric layer wherein said third metal pad is directly above said second metal pad and has the same orientation as said second metal pad;

a fourth dielectric layer, having an opening, formed over said third metal pad wherein said opening in said fourth dielectric layer is formed directly over said third metal pad and exposes part of said third metal pad;

a first number of first via plugs formed between said first metal pad and said second metal pad wherein said first via plugs comprise holes in said second dielectric layer filled with a fourth metal, said first via plugs contact said first metal pad and said second metal pad, and said first number of said first via plugs lie within a first square rotated 45° with respect to said first metal pad; and

a second number of second via plugs formed between said second metal pad and said third metal pad wherein said second via plugs comprise holes in said third dielectric layer filled with a fifth metal, said second vias contact said second metal pad and said third metal pad, said second number of said second via plugs lie within a second square rotated 45° with respect to said third metal pad, and none of said second via plugs are directly above any of said first via plugs.

2. The bond pad structure of claim 1 wherein said first metal pad is AlCu/TiN.

3. The bond pad structure of claim 1 wherein said second metal pad is AlCu/TiN.

4. The bond pad structure of claim 1 wherein said third metal pad is AlCu/TiN.

5. The bond pad structure of claim 1 wherein said fourth metal is tungsten.

6. The bond pad structure of claim 1 wherein said fifth metal is tungsten.

7. The bond pad structure of claim 1 where said first number of first via plugs is between about 70 and 110.

8. The bond pad structure of claim 1 wherein said second number of second via plugs is between about 85 and 135.

9. The bond pad structure of claim 1 wherein said second dielectric layer, said third dielectric layer, and said fourth dielectric are silicon dioxide.

* * * * *